Attorney Docket No. 70010721-2 PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Tan Group Art Unit: 2138

Serial No. 10/606,970 Examiner: Siddiqui, Saqib

Filed: June 25, 2003 Conf. No.: 6461

For: METHOD AND APPARATUS FOR DETECTING AN ERROR IN A BIT SEQUENCE

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

Sir/Madam:

This brief is in furtherance of Applicant's Notice of Appeal filed on December 22, 2006, appealing the decision of the Examiner dated August 23, 2006 finally rejecting claims 1 – 23.

I. Real Party in Interest

The real party in interest in this appeal is Avago Technologies General IP (Singapore) Pte. Ltd., 8 Cross Street, #11-00 PWC Building, Singapore 048424.

II. Related Appeals and Interferences

There are currently no related appeals or interference proceedings in progress that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the present Appeal.

III. Status of Claims

Claims 1 – 22 were originally filed with the application on June 25, 2003. Claims 14 and 22 were amended on June 28, 2006 and claim 23 was added on June 28, 2006. Claims 1 – 23 are pending. Furthermore, no claims have been amended, canceled, or added for purposes of this Appeal.

Claims 1 – 6, 8 – 11, 13 – 18, and 20 – 22 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Gilley (U.S. Pat. No. 6,215,876), in view of Pozidis (U.S. Pub. No. 20030005383), and further in view of Johnson et al. (U.S. Pat. No. 6,587,804, hereinafter Johnson). Claims 7, 12, 19, and 23 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson, and further in view of Yoshimura (U.S. Pat. No. 5,123,020).

This Appeal is made with regard to pending claims 1 – 23.

IV. Status of Amendments

No amendments were filed subsequent to final rejection.

V. Summary of Claimed Subject Matter

According to an embodiment of the invention, as recited in claim 1, a bit error detection circuit (400) comprises a predictor circuit (430) (pg. 8, lines 14 – 21, Fig. 4) that uses a plurality of bits of a bit sequence to predict a next bit in the sequence, a comparator circuit (440) (pg. 8, lines 5 – 29, Fig. 4) that compares an actual next bit in the sequence with the predicted next bit to determine whether there is any error in the actual next bit, and a correction circuit (450) (pg. 10, lines 1 – 9, Fig. 4) that corrects any error in the actual next bit to provide a corrected actual next bit.

According to an embodiment of the invention, as recited in dependent claim 2, the bit error detection circuit of claim 1 comprises a circuit element (462) (pg. 11, lines 1 – 6, Fig. 4) that replaces the actual next bit with the corrected actual next bit in the plurality of bits.

According to an embodiment of the invention, as recited in dependent claim 4, the bit error detection circuit of claim 1 comprises a trigger circuit (460) (pg. 12, lines 26 – 30, Figs. 4, 5) that activates the correction circuit when the predictor circuit contains a plurality of bits in which no erroneous bits have been detected.

According to another embodiment of the invention, as recited in claim 8, a bit error detection circuit (400) comprises a shift register (401, 402, 403, 404, 418, 419, 423) (pg. 8, lines 1 – 7, Fig. 4) that receives N bits of a pseudo-random bit sequence (PRBS), a first logic element (427) (pg. 8, lines 9 – 21) that receives output signals from two stages of the shift register and provides a signal indicative of a predicted (N+1)-th bit, a second logic element (428) (pg. 9, line 1 – 27) that

receives the signal indicative of the predicted (N+1)-th bit and a signal indicative of an actual (N+1)-th bit and provides an output signal indicative of any error in the actual (N+1)-th bit, and a third logic element (462) (pg. 11, lines 1 – 6) that receives the output signal and corrects the actual (N+1)-th bit according to the output signal as the (N+1)-th bit propagates through the shift register.

According to an embodiment of the invention, as recited in dependent claim 9, the third logic element (462) of claim 8 receives the actual (N+1)-th bit from one of the shift register stages, corrects said bit according to the output signal, and inserts said bit as corrected into another one of the shift register stages in place of the actual (N+1)-th bit.

According to an embodiment of the invention, as recited in dependent claim 10, the bit error detection circuit of claim 8 further comprises a trigger circuit (460) (pg. 12, lines 26 – 30, Figs. 4, 5) that activates the third logic element when the shift register contains a bit sequence in which no erroneous bits have been detected.

According to an embodiment of the invention, as recited in dependent claim 13, the bit error detection circuit of claim 8 further comprises a trigger circuit (460) (pg. 12, lines 26 – 30, Figs. 4, 5) that prevents the third logic element from correcting any bits until the shift register contains a bit sequence in which no error has been detected.

According to another embodiment of the invention, as recited in claim 14, a method of detecting errors in a bit sequence comprises predicting (707) (pg. 17, line 29, Fig. 7) a next bit of a bit sequence according to a plurality of previous bits of the sequence, comparing (708) (pg. 17, line 30, Fig. 7) the predicted next bit with an actual next bit, if the comparison indicates a difference between the predicted next bit and the actual next bit, providing an error signal and correcting (704) (pg. 17, line 18, Fig. 7) the actual next bit.

According to another embodiment of the invention, as recited in claim 15, correcting the actual next bit as recited in claim 14 comprises replacing (705) (pg. 17, line 19, Fig. 7) the actual next bit with the corrected actual next bit in the bit sequence.

According to another embodiment of the invention, as recited in claim 17, the method of claim 14 further comprises suppressing (709) (pg. 17, line 30, Fig. 7) any correction of the actual next bit until no error has been detected in a plurality of bits in the sequence.

According to an embodiment of the invention, as recited in claim 21, a bit error detector (400) comprises an actual next bit input (434) that receives a plurality of bits of a bit sequence, a predictor (430) (pg. 8, lines 14 – 21, Fig. 4) coupled to the input and having a predicted next bit output (429), a comparator (440) (pg. 8, line 25 – 29, Fig. 4) coupled to the predicted next bit output and to the actual next bit input, the comparator having an error signal output, and a corrector (450) (pg. 10, lines 1 – 9, Fig. 4) coupled to the error signal output and having a corrected actual next bit output.

According to another embodiment of the invention, as recited in claim 23, a high-speed communications system comprises a pseudo-random bit sequence generator (140) (pg. 1, line 29, Fig. 1) for creating a pseudo-random bit sequence, a transmitter (110) (pg. 1, line 23, Fig. 1) in signal communication with the pseudo-random bit sequence generator, a communications channel (120) (pg. 1, line 25, Fig. 1) in signal communication with the transmitter, the transmitter for transmitting the pseudo-random bit sequence over the communications channel, and a pseudo-random bit sequence error detector (150) (pg. 1, line 29, Fig. 1), in signal communication with the communications channel, for detecting and correcting any error in an actual next bit of the pseudo-random bit sequence, wherein the pseudo-random bit sequence error detector comprises: a predictor circuit (430) (pg. 8, lines 14 – 21, Fig. 4) that uses a plurality of bits of the pseudo-random bit sequence to provide a predicted next bit of the pseudo-random

bit sequence, a comparator circuit (440) (pg. 8, lines 25 – 29, Fig. 4) that compares the actual next bit in the pseudo-random bit sequence with the predicted next bit to determine whether there is an error in the actual next bit; and a correction circuit (450) (pg. 10, lines 1 – 9, Fig. 4) that corrects any error in the actual next bit to provide a corrected actual next bit.

VI. Grounds of Rejection to be Reviewed on Appeal

Whether claims 1 – 6, 8 – 11, 13 – 18, and 20 – 22 are unpatentable under 35 U.S.C. 103(a) over Gilley, in view of Pozidis, and further in view of Johnson and whether claims 7, 12, 19, and 23 are unpatentable under 35 U.S.C. 103(a) over Gilley, in view of Pozidis, and further in view of Johnson, and further in view of Yoshimura.

VII. Argument

In the Final action dated August 23, 2006, the Examiner has rejected claim 1 under 35 U.S.C. 103(a) as allegedly being unpatentable over Gilley, in view of Pozidis, and further in view of Johnson. However, Applicant asserts that claim 1 is not rendered obvious from Gilley in view of Pozidis and Johnson because 1) the Office action has not provided a teaching, suggestion, or motivation to combine Pozidis with Gilley and 2) Gilley teaches away from combining Pozidis with Gilley.

Claim 1

Claim 1 recites:

> "A bit error detection circuit comprising:
> a predictor circuit that uses a plurality of bits of a bit sequence to predict a next bit in the sequence;
> a comparator circuit that compares an actual next bit in the sequence with the predicted next bit to determine whether there is any error in the actual next bit; and
> ***a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit***." (emphasis added)

With regard to claim 1, the Office action states that Gilley teaches the predictor circuit and the comparator circuit, but that Gilley fails to teach the correction circuit. Pozidis is cited for teaching the correction circuit.

Gilley does not provide a teaching, suggestion, or motivation to use a ***correction circuit*** as recited in claim 1

The correction circuit recited in claim 1 is deemed to be taught by Pozidis. As stated in *Ex parte Clapp*, 227 USPQ 972, (Bd. Pat. App. & Inter. 1985) "[t]o support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Additionally, "[t]he examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness." [M.P.E.P. 2142]

Gilley does not expressly or impliedly suggest the claimed invention - The Final action cites Gilley, col. 7, lines 1 – 5 as providing a suggestion to use a correction circuit as taught by Pozidis and as recited in claim 1. At col. 7, lines 1 – 5, Gilley recites:

> "if the number of errors is large (e.g. ≥ 4 bit errors) (66/76), it is concluded that the predicted IV is wrong (76), and appropriate action can be taken (78), which might consist of dropping crypto-sync and attempting to re-acquire it from the received IV (80)."

Although Gilley discloses that "an appropriate action can be taken," nowhere does Gilley expressly or impliedly suggest "a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit" as recited in claim 1. Applicant points out that the test for obviousness in not whether the prior art suggests some alternative action, but whether or not the prior art suggests the claimed invention. The phrase "appropriate action can be taken" is not an express or implied suggestion of the claimed invention, i.e., a correction circuit.

Gilley does teach that an appropriate action may consist of "dropping crypto-sync and attempting to acquire it from the received IV." While Gilley does teach one action that can be taken, nowhere does Gilley expressly or impliedly suggest the claimed invention.

The Final action does not provide a convincing line of reasoning as to why the artisan would have found the claimed invention obvious in light of the teachings of the references - The Final action cites, as support for the combination of Gilley and Pozidis, the conclusory statement:

> "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to use a corrector circuit to correct the bits in Gilley's invention, since one of ordinary skill in the art would have realized that enabling Gilley's invention to correct bits would have made the invention more beneficial and would have allowed Gilley to generate vectors with greater accuracy." (Final action, page 4) (emphasis added)

This conclusory statement is unsupported by any facts. Further, Applicant asserts that the statement does not present a convincing line of reasoning as to why an artisan would have found the claimed invention obvious. The support provided for the Examiner's suggested combination includes the specific statement, "since one of ordinary skill in the art would have realized that enabling Gilley's invention to correct bits would have made the invention more beneficial and would have allowed Gilley to generate vectors with greater accuracy." This statement basically says that an artisan would have selected a correction circuit to make the invention better. Applicant asserts that making an invention better does not provide a fact-based convincing line of reasoning to support a *prima facie* case of obviousness.

Gilley Teaches Away from using a Correction Circuit

Applicant asserts that Gilley teaches away from using a correction circuit and therefore teaches away from the combination of Gilley and Pozidis. As evidence that Gilley teaches away from a correction circuit, Gilley discloses at column 5, lines 21 – 30 that the preferred embodiment achieves a stated objective of maintaining crypto-sync (column 6, line 49) "without error correction." That is, the technique disclosed by Gilley expressly avoids error correction. Applicant asserts that a technique that expressly avoids error correction teaches away from combining Gilley with a reference, such as Pozidis, for its error correction teaching.

Further, in contrast to Applicant's claim 1, Gilley teaches *ignoring* or coasting by the received IV *in the presence of bit errors*. For example, Gilley states:

> "Coasting systems … (a) predict the correct IV, (b) detect if the received IV does not match the predicted IV and, further, (c) if so, ignore or coast by the received IV … . The preferred embodiment therefore utilizes … coasting … in the presence of bit errors to transmitted IV caused by the communications channel … ." (col. 5, lines 20-28)

That is, Gilley teaches ignoring bit errors instead of using *a correction circuit* that *corrects any error* in the actual next bit to provide a *corrected* actual next bit, thereby teaching away from the claimed invention. Teaching away from the claimed invention by a reference is a strong evidence against *prima facie* obviousness.

Dependent claim 2

Claim 2 recites that the correction circuit "comprises a circuit element that ***replaces the actual next bit with the corrected actual next bit*** in the plurality of bits." The limitations of claim 2 are rejected as being taught by Pozidis. The logic for combining Pozidis with Gilley is the same as the logic provided with respect to claim 1. Because of the similarities between the rejections of claims 1 and 2, Applicant asserts that the remarks provided above with respect to claim 1 apply also to claim 2.

Dependent claim 3

Dependent claim 3 is dependent on claim 1. Applicant asserts that claim 1 is allowable at least based on an allowable claim 1.

Dependent claim 4

Claim 4 recites that the bit error detection circuit of claim 1 further includes "***a trigger circuit that activates the correction circuit when the predictor circuit contains a plurality of bits in which no erroneous bits have been detected***." The support in the Final action for the rejection of claim 4 is "(Figure 4 #68, columns 6, lines 46 – 57, it should be noted that the Figure 4 #64, will trigger the correction circuit which will be placed at Figure 4 #78)." (Final action, page 6) Applicant asserts that Gilley does not teach or suggest a correction circuit and Gilley explicitly states that the preferred embodiment achieves the stated objective of maintaining crypto-sync "without error correction." Because Gilley does not teach or suggest error correction, it follows that a trigger circuit that activates a correction circuit is not taught or suggested by Gilley.

In the Final action, Fig. 4, #68 and column 6, lines 46 – 57 of Gilley are cited as teaching the limitations of claim 4. Elements 64, 66, and 68 of Fig. 4 teach that when no bit errors are detected, it should be assumed that the received and predicted initialization vectors are correct (elements 68 and 72). These elements, particularly element 68, teach nothing about a trigger circuit that "activates the correction circuit when the predictor circuit contains a plurality of bits in which no erroneous bits have been detected" as recited in claim 4.

Dependent claims 5, 6, and 7

Dependent claims 5, 6, and 7 include limitations related to the trigger circuit recited in claim 4. Because, as described above, Gilley does not disclose a correction circuit or a trigger circuit that activates the correction circuit, Applicant asserts that Gilley does not teach or suggest the limitations related to the trigger circuit.

Claim 8

Claim 8 recites:

> "A bit error detection circuit comprising:
> a shift register that receives N bits of a pseudo-random bit sequence (PRBS);
> a first logic element that receives output signals from two stages of the shift register and provides a signal indicative of a predicted (N+1)-th bit;
> a second logic element that receives the signal indicative of the predicted (N+1)-th bit and a signal indicative of an actual (N+1)-th bit and provides an output signal indicative of any error in the actual (N+1)-th bit; and
> a third logic element that receives the output signal and corrects the actual (N+1)-th bit according to the output signal as the (N+1)-th bit propagates through the shift register. " (emphasis added)

Claim 8 is rejected under the same logic as claim 1. Because of the similarities between claims 1 and 8, Applicant asserts that the remarks provided above with reference to claim 1 apply also to claim 8.

Dependent claims 9 – 13

Dependent claim 9 has similar limitations to dependent claim 2 and therefore the remarks provided above with reference to claim 2 apply also to claim 9.

Dependent claim 10 has similar limitations to dependent claim 4 and therefore the remarks provided above with reference to claim 4 apply also to claim 10.

Dependent claims 11 and 12 include limitations related to the trigger circuit recited in claim 10. Because, as described above, Gilley does not disclose correction logic or a trigger circuit that activates the correction logic, Applicant asserts that Gilley does not disclose the limitations related to the trigger circuit.

Dependent claim 13 has similar limitations to dependent claim 4 and therefore the remarks provided above with reference to claim 4 apply also to claim 13.

Claims 14, 21, and 22

Claims 14, 21, and 22 include limitations that are similar to the limitations in claim 1. These claims are rejected under the same logic as claim 1. Because of the similarities between claims 1 and claims 14, 21, and 22, Applicant asserts that the remarks provided above with reference to claim 1 apply also to these claims.

Dependent claims 15 – 20

Dependent claim 15 has similar limitations to dependent claim 2 and therefore the remarks provided above with reference to claim 2 apply also to claim 15.

Dependent claim 17 has similar limitations to dependent claim 4 and therefore the remarks provided above with reference to claim 4 apply also to claim 17.

Dependent claims 16 and 18 – 20 are dependent on claim 14. Applicant asserts that these claims are allowable at least based on an allowable claim 14.

Independent claim 23

Independent claim 23 includes limitations similar to claim 1. Because of the similarities between claims 1 and 23, Applicant asserts that the remarks provided above with reference to claim 1 apply also to claim 23.

SUMMARY

The claimed invention is a bit error detector that includes a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit. In contrast to the claimed invention, the prior art does not teach or suggest a bit error detector that includes a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit.

For all the foregoing reasons, it is earnestly and respectfully requested that the Board of Patent Appeals and Interferences reverse the rejections of the Examiner regarding claims 1 – 23, so that this case may be allowed and pass to issue in a timely manner.

Respectfully submitted,
Tong Tee Tan et al.

Date: July 6, 2007 By: /mark a. wilson/

Mark A. Wilson
Registration No. 43,994

Wilson & Ham
PMB: 348
2530 Berryessa Road
San Jose, California 95132

Telephone: (925) 249-1300
Fax: (925) 249-0111

VIII. Claims Appendix

1. A bit error detection circuit comprising:

a predictor circuit that uses a plurality of bits of a bit sequence to predict a next bit in the sequence;

a comparator circuit that compares an actual next bit in the sequence with the predicted next bit to determine whether there is any error in the actual next bit; and

a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit.

2. A bit error detection circuit as in claim 1 wherein the correction circuit comprises a circuit element that replaces the actual next bit with the corrected actual next bit in the plurality of bits.

3. A bit error detection circuit as in claim 1 wherein the bit sequence comprises a pseudo-random bit sequence and the predictor circuit predicts the next bit by comparing two of the bits of the sequence.

4. A bit error detection circuit as in claim 1 and further comprising a trigger circuit that activates the correction circuit when the predictor circuit contains a plurality of bits in which no erroneous bits have been detected.

5. A bit error detection circuit as in claim 4 wherein the trigger circuit activates the correction circuit when no erroneous bits have been observed during a predefined interval.

6. A bit error detection circuit as in claim 5 wherein the predefined interval is defined in terms of a quantity of bits.

7. A bit error detection circuit as in claim 5 wherein the predefined interval is defined in terms of an interval of time.

8. A bit error detection circuit comprising:

a shift register that receives N bits of a pseudo-random bit sequence (PRBS);

a first logic element that receives output signals from two stages of the shift register and provides a signal indicative of a predicted (N+1)-th bit;

a second logic element that receives the signal indicative of the predicted (N+1)-th bit and a signal indicative of an actual (N+1)-th bit and provides an output signal indicative of any error in the actual (N+1)-th bit; and

a third logic element that receives the output signal and corrects the actual (N+1)-th bit according to the output signal as the (N+1)-th bit propagates through the shift register.

9. A bit error detection circuit as in claim 8 wherein the third logic element receives the actual (N+1)-th bit from one of the shift register stages, corrects said bit according to the output signal, and inserts said bit as corrected into another one of the shift register stages in place of the actual (N+1)-th bit.

10. A bit error detection circuit as in claim 8 and further comprising a trigger circuit that activates the third logic element when the shift register contains a bit sequence in which no erroneous bits have been detected.

11. A bit error detection circuit as in claim 10 wherein the trigger circuit comprises a logic circuit that receives the output signal and provides an enabling signal if no error is indicated while a predefined number of bits propagates through the shift register.

12. A bit error detection circuit as in claim 10 wherein the trigger circuit comprises a timer that provides an enabling signal if no error is indicated during a predefined time interval.

13. A bit error detection circuit as in claim 8 and further comprising a trigger circuit that prevents the third logic element from correcting any bits until the shift register contains a bit sequence in which no error has been detected.

14. A method of detecting errors in a bit sequence comprising:

predicting a next bit of a bit sequence according to a plurality of previous bits of the sequence;

comparing the predicted next bit with an actual next bit; and

if the comparison indicates a difference between the predicted next bit and the actual next bit, providing an error signal and correcting the actual next bit.

15. A method as in claim 14 wherein correcting the actual next bit comprises replacing the actual next bit with the corrected actual next bit in the bit sequence.

16. A method as in claim 14 wherein the bit sequence comprises a pseudo-random bit sequence.

17. A method as in claim 14 and further comprising suppressing any correction of the actual next bit until no error has been detected in a plurality of bits in the sequence.

18. A method as in claim 14 and further comprising determining whether any bit errors are detected during a predefined interval.

19. A method as in claim 18 and further comprising measuring a period of time to determine when the predefined interval has elapsed.

20. A method as in claim 18 and further comprising counting a predefined number of bits as they propagate through a circuit element to determine when the predefined interval has elapsed.

21. A bit error detector comprising:

an actual next bit input that receives a plurality of bits of a bit sequence;

a predictor coupled to the input and having a predicted next bit output;

a comparator coupled to the predicted next bit output and to the actual next bit input, the comparator having an error signal output; and

a corrector coupled to the error signal output and having a corrected actual next bit output.

22. A bit error detector as in claim 21 wherein:

the predictor comprises a predictor circuit for receiving the plurality of bits, for determining a predicted next bit from at least some of the plurality of bits, and for providing the predicted next bit at the predicted next bit output;

the comparator comprises a comparator circuit for receiving the predicted next bit and the actual next bit, for comparing the predicted next bit and the actual next bit, and for providing an error signal at the error signal output when a difference is detected between the predicted next bit and the actual next bit; and

the corrector comprises a correction circuit for receiving the error signal, producing a corrected actual next bit, and providing the corrected actual next bit at the corrected actual next bit output.

23. A high-speed communications system, comprising:

a pseudo-random bit sequence generator for creating a pseudo-random bit sequence;

a transmitter in signal communication with the pseudo-random bit sequence generator;

a communications channel in signal communication with the transmitter, the transmitter for transmitting the pseudo-random bit sequence over the communications channel; and

a pseudo-random bit sequence error detector, in signal communication with the communications channel, for detecting and correcting any error in an actual next bit of the pseudo-random bit sequence, wherein the pseudo-random bit sequence error detector comprises:

a predictor circuit that uses a plurality of bits of the pseudo-random bit sequence to provide a predicted next bit of the pseudo-random bit sequence;

a comparator circuit that compares the actual next bit in the pseudo-random bit sequence with the predicted next bit to determine whether there is an error in the actual next bit; and

a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit.

IX. Evidence Appendix

NONE

X. Related Proceedings Appendix

NONE